Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.040”**

**ANODE**

**.032 x .032”**

**.040”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .032 X .032”**

**Backside Potential: CATHODE**

**Mask Ref: TRJ**

**APPROVED BY: DK DIE SIZE .040” X .040” DATE: 10/21/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .010” P/N: 1N4003**

**DG 10.1.2**

#### Rev B, 7/1